IN THE CLAIMS

1. (Currently amended) A circuit device comprising: a first delay circuit, a second delay circuit, and a third delay circuit, each for outputting data in response to a pulse of a clock signal, the first, second and third delay circuits being serially coupled; ~~and~~ a signal processing circuit for processing said outputted data from said first delay circuit, ~~a signal processing circuit comprising a second delay circuit for outputting data in response to said pulse of said clock signal, wherein said circuit device comprises~~; and a control circuit for controlling whether said second delay circuit and said third delay circuit should be supplied with said pulse of said clock signal on the basis of whether outputted data from said first delay circuit in response to said pulse of said clock signal is equal to data to be outputted from said first delay circuit in response to the next pulse.

2. (Canceled)

3. (Currently amended) A circuit device as claimed in claim 2, wherein each of said ~~at least two second~~ delay circuits comprises a plurality of data inputting portions for receiving data and a plurality of data outputting portions for outputting data.

4. (Canceled)

5. (Canceled)

6. (Previously presented) A circuit device as claimed in claim 1, wherein said control circuit comprises: a deciding circuit for deciding whether said second delay circuit should be supplied with said pulse of said clock signal on the basis of whether said outputted data from said first delay circuit in response to said pulse of said clock signal is equal to said data to be outputted from said first delay circuit in response to the next pulse; and a clock driver for allowing or blocking supply of said pulse of said clock signal to said second delay circuit in accordance with a decision of said deciding circuit.

7. (Previously presented) A circuit device as claimed in claim 6, wherein said deciding circuit comprises: a judging section for judging whether said outputted data from said first delay circuit in response to each pulse of said clock signal is equal to said data to be outputted in said first delay circuit in response to the next pulse, a counter for incrementing a count value when said judging section judges both data to be equal and resetting a counter value when said judging section judges both data not to be equal; and a control signal generating section for comparing said count value with a comparison value to obtain a comparison result and for outputting, on the basis of said comparison result, a pulse supply controlling signal representing whether said second delay circuit should be supplied with said pulse of said clock signal.

8. (Previously presented) A circuit device as claimed in claim 7, wherein said comparison value corresponds to a total number of said second delay circuits.

9. (Previously presented) A circuit device as claimed in claim 1, wherein each of said first delay circuits and second delay circuits is constructed by one or more D flip-flops.